Junctionless Ge MOSFETs Fabricated on 10 nm-thick GeOI Substrate

D. D. Zhao[a,b,c], T. Nishimura[a,b], C. H. Lee[a,b], R. Ifuku[a], K. Nagashio[a,b], K. Kita[a,b], and A. Toriumi[a,b]

[a] Department of Materials Engineering, The University of Tokyo, 7-3-1 Hongo, Tokyo 113-8656, Japan
[b] JST-CREST, 7-3-1 Hongo, Tokyo 113-8656, Japan
[c] College of Nuclear Science and Technology, Beijing Normal University, Beijing 100875, China

Junctionless field-effect transistor (FET) has recently been proposed for Si nanowire FETs. It avoids junction formation process and shows less sensitive to the channel interface. Here, we demonstrate junctionless FET fabricated on 11 nm-thick heavily doped p-type Ge-on-insulator (GeOI) substrate which combines the higher hole mobility in Ge than in Si with all junctionless FET advantages. The device shows similar I-V characteristics with conventional FETs, and the I_{on}/I_{off} ratio is larger than 10^4. In addition, the field effect mobility seems to be rather flat with regard to the carrier density. What's more, the Ge junctionless p-FET has better doping flexibility thanks to the strong Fermi level pinning at metal/Ge interface.

Introduction

In the field of microelectronics, in order to continue Moore's law, new materials and new architectures are required. Recently, junctionless FET has been reported for Si nanowire FETs on Si-on-insulator (SOI) substrate (1). It avoids junction formation process and the doping concentration is constant throughout the device. Compared with conventional FETs, the junctionless FET shows less sensitive to the channel interface. However, the devices need to be fabricated on heavily doped SOI with the impurity concentration typically ranging from 10^{19} to 10^{20} cm^{-3} and a comparatively low mobility was expected.

On the other hand, Germanium (Ge) has been drawing interest in the last few years as a promising alternative to Silicon because of its intrinsic higher carrier mobility (2-4). Ge-on-insulator (GeOI), which combines the higher carrier mobility in Ge than in Si with the better electrostatic channel control of fully-depleted metal-oxide-semiconductor field-effect transistor (MOSFET) technology, has been widely reported on the performance and scalability of Ge pMOSFETs (3-10) , comfirming it an attractive integration platform for future IC technology.

In this work, we demonstrate junctionless FET fabricated on GeOI substrate. The current-voltage (I-V) characteristics and the field effect mobility are investigated. The opportunity and prospects of this device are also discussed.

Device fabrication

Heavily doped p-type GeOI wafer with 100 nm-thick buried SiO_2 was used. **Figure 1**

shows the dopant profile in GeOI substrate by secondary ion mass spectroscopy (SIMS), which indicates that the substrate doping concentration is around 10^{19} cm^{-3}. First, The initial 100 nm Ge film was thinned by a careful wet etching process. The final thickness of Ge film was about 11.5 nm, which was determined by spectroscopic ellipsometry. Next, mesa type Ge island with local narrow channel (~0.16 μm) was defined by e-beam lithography and photo lithography. After methanol, HCl cleaning process, Ni was deposited by e-beam evaporation and then was patterned by the lift-off process, followed by annealing at 400°C for 5 min in N_2 ambient. Finally, Al was deposited as backgate electrode.

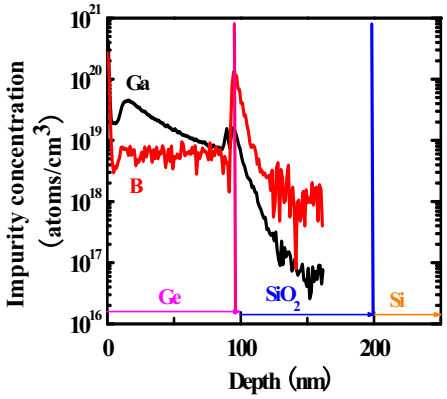


Figure 1 Impurity profile in heavily doped GeOI substrate by SIMS, the doping concentration of the GeOI substrate is around 10^{19} cm^{-3}.

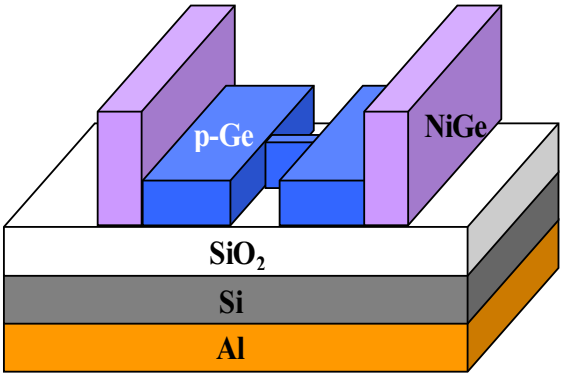
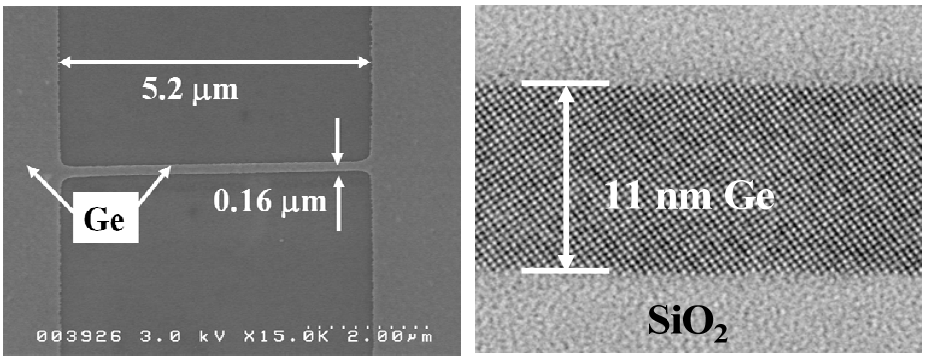


Figure 2 A schematic cross-sectional view of the junctionless Ge MOSFET structure.

Results and discussion

Figure 2 show a schematic cross-sectional view of the junctionless Ge MOSFET structure studied in this paper. **Figure 3 (a) and (b)** show a SEM image of the locally narrowed channel and a XTEM image of cross-sectional GeOI respectively. The Ge is only 11 nm and still keeps good crystalline quality after the thinning process. X-ray diffraction pattern for as-deposited and annealed Ni/GeOI samples are shown in **Fig.4**. The initial Ni thickness was 48 nm, which was determined by grazing incidence X-ray reflectometry (GIXR). The initial Ni (111) peak at $2\theta = 45°$ completely disappears after annealing, indicating a complete reaction of the Ni film with Ge. A sharp peak at $2\theta =$

46° is observed after annealing the sample in N_2 ambient at 400°C for 5 min. The peak was identified as NiGe (220) (11), which indicates that NiGe S/D electrodes were formed after annealing.



(a) (b)

Figure 3 (a) A SEM image of the locally narrowed channel. (b) A XTEM image of cross-sectional GeOI. The Ge is only 11 nm and still keeps good crystalline quality after the thinning process.

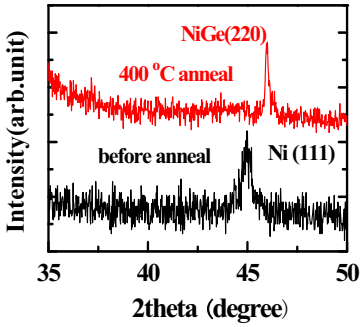
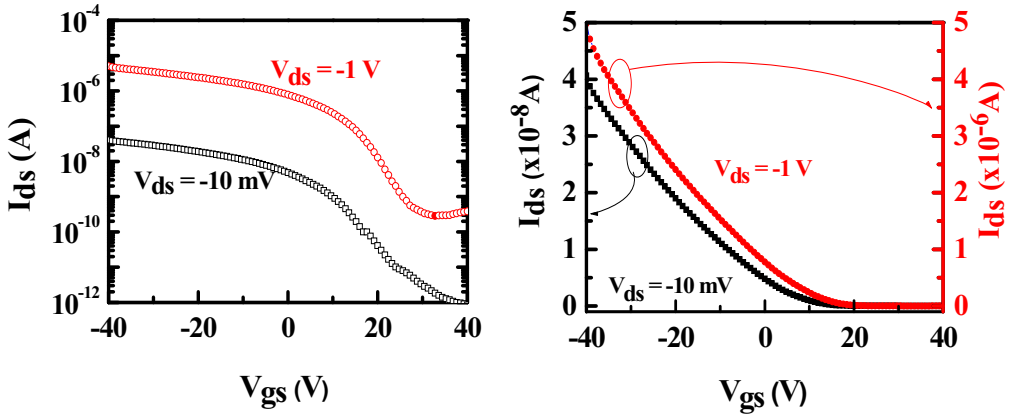


Figure 4 X-ray diffraction pattern for both as-deposited and annealed Ni/ GeOI samples. The 48 nm Ni completely reacted with Ge and NiGe was formed after annealing.

Figure 5 shows the I_{ds}-V_{gs} characteristics of the junctionless Ge device shown in Fig.3 at V_{ds} = -10 mV and V_{ds} = -1 V, which is almost the same as the conventional ones. The I_{on}/I_{off} ratio of the device is larger than 10^4 between V_{gs} = -40 V and V_{gs} = 40 V. In the junctionless MOSFET, carriers are located inside Ge film, and the channel is a resistor without the gate bias. By applying a negative gate bias, the hole accumulation layer is formed at the interface and the majority carriers flow both at the interface and in the bulk. When a positive gate bias is applied, majority carriers are electrostatically depleted, and drain current is decreased. Therefore, the depletion layer width is a critical parameter for this junctionless FET to achieve the off-state. By the simple depletion layer approximation, the relationship between the maximum depletion layer width W_m and the impurity concentration N_A can be expressed as

$$W_m = \sqrt{\frac{4\varepsilon_s kT \ln(N_A/n_i)}{q^2 N_A}}, \quad (1)$$

where k, q, ε_s, n_i are the Boltzmann constant, the elementary charge, the permittivity of the semiconductor, and the intrinsic carrier concentration of the semiconductor, respectively (12). The dielectric constant and intrinsic carrier concentration of Ge is 16.0 and 2.4 $\times 10^{13}$ cm^{-3}, respectively. So the maximum depletion layer width is estimated to be 11 nm when the substrate impurity concentration is around 10^{19} cm^{-3}. Thus, by reducing the Ge thickness to be thinner than its maximum depletion layer width so as to fully deplete the channel of carriers, we could successfully turn off the device.



(a) (b)

Figure 5 I_{ds}-V_{gs} characteristics at V_{ds}= -10 mV and -1 V of the FET shown in Fig.3. The GeOI substrate doping concentration N_A is around $10^{19}cm^{-3}$. I_{on}/I_{off} ratio is roughly 10^4 at V_{ds}= -1V. (a) subthreshold, and (b) linear charactersitics.

The field effect mobility can be estimated as follows.

$$\mu = \frac{L}{W}\frac{I_{ds}}{V_{ds}}\frac{1}{Q}, \quad (2)$$

$$Q = qN_s = \int_{-\infty}^{V_{gs}} C_{gc} dV_{gs}, \quad (3)$$

$$\frac{1}{C_{gc}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}. \quad (4)$$

In the present 11-nm thick Ge junctionless FET, the capacitance of SiO_2 is much smaller than the capacitance of the Ge depletion layer, so carrier density N_s can be approximated by

$$N_s = Q/q = C_{ox}(V_{gs} - V_{th})/q. \quad (5)$$

Here, V_{th} is the threshold voltage and was estimated from g_m-V_{gs} characteristics. C_{ox} was estimated by the saturated capacitance-voltage (C-V) curve between the back-gate and S/D electrodes in the negative bias condition. The parasitic capacitance was well subtracted by using two devices with different gate length (L_1=100 μm, W_1=130 μm, L_2=200 μm, W_2=130 μm), and C_{ox} was estimated to be 3.23×10^{-8} F/cm^2. Using Eqs.(2) and (5), we can approximately estimate the hole mobility, and the result is shown in **Fig.**

6. Si universal mobility is also shown for comparison. The mobility of junctionless Ge p-MOSFET at N_A~$10^{19}cm^{-3}$ is around 110 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and is higher than Si universal mobility at N_A=6.6*$10^{17}cm^{-3}$ even though the substrate doping concentration is much higher than the Si one. In addition, our Ge junctionless device is not well optimized and the Si substrate capacitance should be considered in more accurate analysis, so the mobility of junctionless Ge MOSFET in Fig.6 is actually underestimated since N_s is overestimated. What's more, the mobility of junctionless Ge MOSFET seems to be rather flat with regard to the areal carrier density, N_s. In conventinal inversion-mode MOSFETs, the minority carriers are accumulated at the semiconductor/insulator interface, they are necessarily scattered by the interface roughness and/or by charges trapped in the insulator or at the interface. As N_s increases, the scattering events also increase and thus the carrier mobility decreases. In the junctionless Ge MOSFET, however, majority carriers are located inside the Ge film, and comparatively less sensitive to the interface. When the device is turned on, the whole Ge film acts as the channel like a resistor, thus the mobility seems to be rather flat with carrier density.

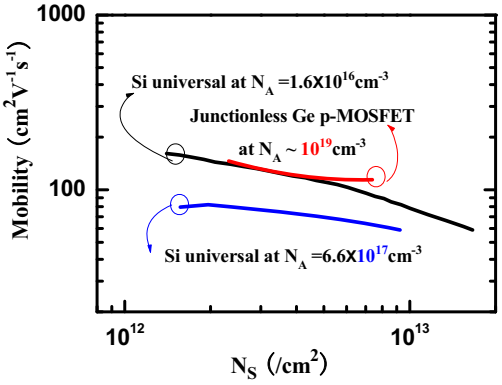
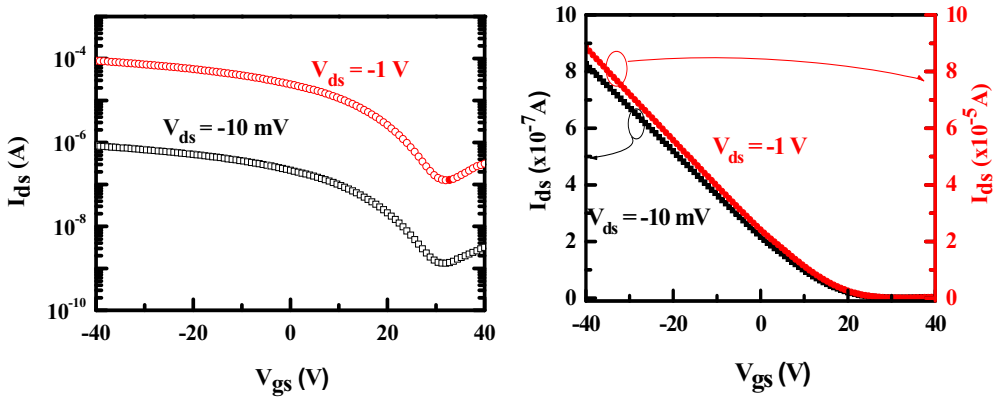


Figure 6 The field effect mobility of the 11 nm-thick Ge junctionless FET at V_{ds} = -10 mV. Si universal mobility is shown for comparison. The mobility of the junctionless Ge FET at N_A ~ 10^{19} cm^{-3} is higher than Si universal mobility at N_A= 6.6x10^{-17} cm^{-3}. In addition, the mobility seems to be rather flat with regard to the carrier density.

The key challenge of the Ge junctionless FETs is to make the ultra thin Ge film, because the most important point is to fully deplete majority carriers in the heavily-doped channel for the off-state. Although nanowire would be better for cutting-off the current thanks to the better electric confinement (1), rather wide channel FETs were controllable in 10 nm-thick Ge case in the present experiment. In further reduction of the Ge thickness, however, the channel current was unstable possibly due to the nonuniformity of Ge thickness.

In the case of Si junctionless MOSFETs, the SOI substrate needs to be heavily doped to make the ohmic contact. While in Ge case, any metals/ p-Ge contacts show ohmic behaviour because the Fermi level at metal/Ge interface is strongly pinned near the valence band edge of Ge (13). Thus, it is worth while mentioning the junctionless Ge p-MOSFET in particular has better flexibility against the doping density in Ge, which means that lightly doped thin Ge film on insulator will also be usable for p-type junctionless FETs. In fact, we also successfully fabricated junctionless Ge p-MOSFET

using lightly p-doped (~10^{16} cm^{-3}) GeOI substrate. The Ge and BOX SiO_2 thickness was 30 nm and 400 nm respectively. The I_{ds}-V_{gs} characteristics are shown in **Fig.7**. Since the impurity concentration is reduced, the maximum depletion layer thickness is increased, thus even though the Ge thickness is increased to 30 nm, we can still cut off the device as shown in Fig.7. In other words, in the lightly doped case, the moderately thick Ge can be used. As a result, the substrate thickness variation can be degraded. The I_{ds}-V_{gs} characteristics comparison of the devices using heavily doped GeOI and lightly-doped GeOI is shown in **Fig.8**. The current is normalized by SiO_2 thickness, channel length and channel width. The slope is corresponded to the mobility, we can see the mobility is enhanced when the doping concentration is decreased.



(a) (b)

Figure 7 I_{ds}-V_{gs} characteristics at V_{ds}= -10 mV and -1 V of the junctionless FET using lightly doped GeOI substrate, the doping concentration N_A is around 10^{16} cm^{-3}. The channel length and channel width is 100 μm and 130 μm respectively. I_{on}/I_{off} ratio is roughly 10^3 at V_{ds}= -10 mV. (a) subthreshold, and (b) linear charactersitics.

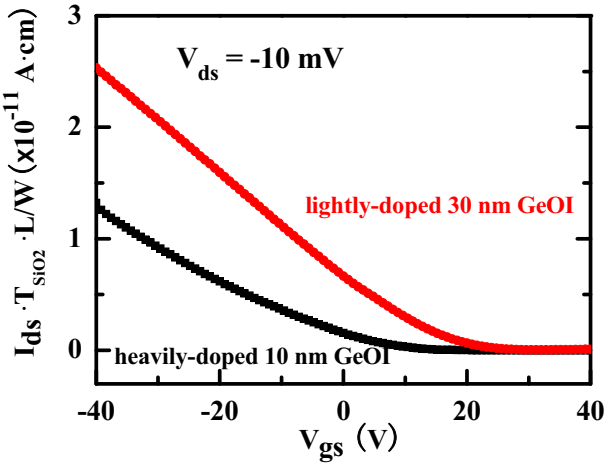


Figure 8 The I_{ds}-V_{gs} characteristics comparison of the devices using heavily doped (N_A ~ 10^{19} cm^{-3}) GeOI and lightly-doped (N_A ~ 10^{16} cm^{-3}) GeOI. The slope is corresponded to the mobility, and the mobility is enhanced when the substrate doping concentration is decreased.

Conclusion

In summary, we have proposed and demonstrated junctionless Ge p-MOSFETs on the ultra-thin GeOI. Higher carrier mobility in Ge than in Si suggests that Ge will be more appropriate for junctionless MOSFETs. Lightly doped GeOI substrates can also be used for junctionless p-MOSFETs in particular thanks to the strong Fermi level pinning at metal/Ge contact. This is another advantage of Ge junctionless p-MOSFET over Si one. We think it will surmount the performance limit of Si MOSFETs.

Acknowledgments

D. D. Zhao and C. H. Lee are grateful for the financial supports by China Scholarship Council and the MEXT of Japan, respectively.

References

1. J.-P. Colinge, C.W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. ONeill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy: Nature Nanotech. **5** (2010) 225.
2. T. Yamamoto, Y. Yamashita, M. Harada, N. Taoka, K. Ikeda, K. Suzuki, O. Kiso, N. Sugiyama, and S. Takagi, Tech. Dig. IEDM (2007) 1041.
3. J. Mitard, B. De Jaeger, F.E. Leys, G. Hellings, K. Martens, G. Eneman, D.P. Brunco, R. Loo, J.C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C.H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, M.M. Heyns, Tech. Dig. IEDM (2008) 873.
4. C.H. Lee, T. Nishimura, T. Tabata, S.K. Wang, K. Nagashio, K. Kita, and A. Toriumi,Tech. Dig. IEDM (2010) 416.
5. K. Romanjek, L. Hutin, C. Le Royer, A. Pouydebasque, M.-A. Jaud, C. Tabone, E. Augendre, L. Sanchez, J.-M. Hartmann, H. Grampeix, V. Mazzocchi, S. Soliveres, R. Truche, L. Clavelier, P. Scheiblin, X. Garros, G. Reimbold, M. Vinet, F. Boulanger, and S. Deleonibus: in Proc. ESSDERC, 2008, p. 75.
6. L. Hutin, C. Le Royer, J.-F. Damlencourt, J.-M. Hartmann, H. Grampeix, V. Mazzocchi, C. Tabone, B. Previtali, A. Pouydebasque, M. Vinet, and O. Faynot: IEEE Electron Device Lett. 31 (2010) 234.
7. C. Le Royer, B. Vincent, L. Clavelier, J.-F. Damlencourt, C. Tabone, P. Batude, D. Blachier, R. Truche, Y. Campidelli, Q. T. Nguyen, S. Cristoloveanu, S. Soliveres, G. Le Carval, F. Boulanger, T. Billon, D. Bensahel, and S. Deleonibus: IEEE Electron Device Lett. 29 (2008) 635.
8. J. Feng, G. Thareja, M. Kobayashi, S. Chen, A. Poon, Y. Bai, P. B. Griffin, S. S.Wong, Y. Nishi, and J. D. Plummer: IEEE Electron Device Lett. 29 (2008) 805.
9. T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.-M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure: Mater. Sci. Semicond. Process. 9 (2006) 444.

10. M.Vinet, C. Le Royer, P. Batude, J.-F. Damlencourt, J.-M. Hartmann, L.Hutin, K. Romanjek, A. Pouydebasque, and O. Thomas: Int. J. Nanotechnology. 7 (2010) 304.
11. H. Pfisterer and K. Schubert: Z. Metallkd. **41** (1950) 358.
12. S. M. Sze: *Physics of Semiconductor Devices* (Wiley, New York, 1981) 2nd ed., pp. 373.
13. T. Nishimura, K. Kita, and A. Toriumi: Appl. Phys. Lett. **91** (2007) 123123.